Listing of the Claims

This listing of claims will replace all prior versions and listings of claims in the application.

1   1.   A processing apparatus for video and or audio signals comprising:
2   a first module (11) having a controller (13C) coupled to a signal processor (13A)
3   having a signal processing characteristic selected from a plurality signal processing
4   characteristics stored in a non-volatile memory (13B); and,
5   a second module (21) coupled to said first module (11) and having a specific input
6   output signal coupling characteristic,
7   wherein said controller (13C) determines said input output signal coupling
8   characteristic of said second module (21) and in accordance therewith selects from said
9   plurality signal processing characteristics stored in said non-volatile memory (13B) a
10   signal processing characteristic for said signal processor(13A).

1   2.   The apparatus of claim 1, wherein said controller (13C) determines said input
2   output signal coupling characteristic of said second module (21) during a power up
3   sequence.

1   3.   The apparatus of claim 1, wherein said second module (21) comprises a
2   personality pin (PERP) coupled to said first module (11) to enable detection of said input
3   output signal coupling characteristic by said controller (13C).

1   4.   The apparatus of claim 1, wherein said controller (13C) determines said input
2   output signal coupling characteristic of said second module (21) by measurement of a
3   coupling node.

1   5.   The apparatus of claim 1, wherein said controller (13C) determines said input
2   output signal coupling characteristic of said second module (21) in accordance with a
3   potential at a node between said first and second module.

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1   6.   The apparatus of claim 1, wherein said controller (13C) determines said input

2   output signal coupling characteristic of said second module (21) by measurement and

3   comparison with a lookup table.

1   7.   The apparatus of claim 1, wherein said second module (21) comprises only

2   passive electronic circuitry.

1   8.   The apparatus of claim 1, wherein other ones of said plurality signal processing

2   characteristics stored in said non-volatile memory (13B) correspond with other ones of

3   said second module (21) each having different input output signal coupling

4   characteristics.

1   9.   The apparatus of claim 1, wherein said second module (21) comprises passive and

2   active electronic circuitry.

1   10.   The apparatus of claim 9, wherein said active electronic circuitry is functionally

2   configurable.

1   11.   The apparatus of claim 1, wherein said first module (11) has an audio signal

2   processing characteristic.

1   12.   A processing apparatus for video and or audio signals, comprising:

2   a first module having a controller (13C) coupled to a memory (13B) and to a

3   signal processor (13A) having a signal processing characteristic determined by one of a

4   plurality of processing characteristics stored in said memory (13B); and,

5   a second module (21) having a second signal processing characteristic;

6   wherein said controller (13C) determines said second signal processing

7   characteristic of said second module (21) and retrieves from said plurality of processing

8   characteristics stored in said memory (13B) a processing characteristic for said signal

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9   processor (13A) in accordance with said determined signal processing characteristic of

10 said second module (21).

1   13.   The apparatus of claim 12, wherein other ones of said plurality processing

2   characteristics stored in said memory (13B) correspond with other ones of said second

3   module (21) each having a different signal processing characteristic.

1   14.   The apparatus of claim 12, wherein said controller (13C) determines said signal

2   processing characteristic of said second module (21) by measurement of a second module

3   identifier (ZR) during a power up sequence.

1   15.   A processing apparatus for video and or audio signals comprising:

2   a network interface (300);

3   a controller (13C) coupled to said network interface(300);

4   a memory (13B) coupled to said controller(13C); and,

5   a signal processor (13A) coupled to said memory(13C), said signal processor

6   (13A) having a signal processing characteristic determined in accordance with a

7   characteristic stored in said memory (13B),

8   where in accordance with a signal (RC1)from said network interface (300), said

9   controller (13C) accesses from a plurality of characteristics stored in said memory (13B)

10 a characteristic specific to said processing apparatus.

1   16.   The apparatus of claim 15, wherein access to ones of said stored plurality of

2   signal processing characteristics is limited to only said specific characteristic.

1   17.   The apparatus of claim 15, wherein said plurality of characteristics stored in said

2   memory (13B) enable differing levels of signal processing complexity by said signal

3   processor (13A).

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1   18.   The apparatus of claim 15, wherein access to ones of said stored plurality of

2   signal processing characteristics is in accordance with said processing apparatus selling

3   price.

1   19.   The apparatus of claim 15, where in accordance with a second signal (RC2) from

2   said network interface (300) said controller (13C) enables unlimited access to ones of

3   said stored plurality of signal processing characteristics.

1   20.   The apparatus of claim 15, wherein said memory (13B) containing said plurality

2   of signal processing characteristics is alterable in accordance with a second signal (RC2)

3   from said network interface (300).

1   21.   A method for configuring a multi-function signal processing apparatus for users

2   requiring less than all available functions, comprising the steps of:

3   storing a signal processing characteristic for each of said available functions; and,

4   enabling access to at least a predetermined one of said plurality of signal

5   processing characteristics, all remaining ones of said plurality of signal processing

6   characteristics being non-accessible,

7   subsequent to said storing and enabling steps said signal processing apparatus

8   being operable only with said at least predetermined one of said plurality of signal

9   processing characteristics.

1   22.   The method of claim 21, comprising the step of:

2   implementing said enabling step in a field programmable gate array (13A).

1   23.   The method of claim 21, wherein said enabling step comprises the step of

2   inhibiting access to all but said at least predetermined one of said plurality of signal

3   processing characteristics.

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1   24.   The method of claim 21, wherein said enabling step comprises the step of

2   enabling said at least predetermined one of said plurality of signal processing

3   characteristics to be read during a power up condition of said apparatus.

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